respective metal wires connecting the tips of the LOC inner leads to electrode pads on the semiconductor chip and tips of the standard inner leads to electrode pads on the semiconductor chip,

a sealing resin encapsulating the semiconductor chip, the die pad, the tips of the LOC and the standard inner leads, and the metal wires, and

respective outer leads extending successively from the LOC inner leads and the standard inner leads and protruding outwardly from the sealing resin, wherein the LOC inner leads and the standard inner leads are co-planar.

3. (Twice Amended) The semiconductor package of claim 2, wherein a clearance between the LOC inner leads and the die pad is larger than total thickness of the semiconductor chip and the die bond material.

6. (Twice Amended) A semiconductor package comprising:

a semiconductor chip,

a die pad,

a die bonding material fixing the semiconductor chip to the die pad,

lead-on-chip (LOC) inner leads having tips spaced from and extending across the semiconductor chip,

standard inner leads,

respective metal wires connecting the tips of the LOC inner leads to electrode pads on the semiconductor chip and tips of the standard inner leads to electrode pads on the semiconductor chip,

a sealing resin encapsulating the semiconductor chip, the tips of the LOC and the standard inner leads, and the metal wires, and

respective outer leads extending successively from the LOC inner leads and the standard inner leads and protruding outwardly from the sealing resin, wherein

a distance between upper surfaces of the outer leads and an upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and a lower surface of the sealing resin, and

ends of the die pad are exposed at opposed side surfaces of the sealing resin and lie in a plane parallel to a plane in which the outer leads protrude.